Amendment in the Claims

1. (Currently Amended) A processor, comprising:

a Boolean logic unit formed in a static circuit with a static data path, wherein the Boolean logic unit is operable for dynamically performing the short-circuit evaluation of a Conjunctive Normal Form Boolean expressions/operations in an instruction store without further compilation or optimization of the expression by the Boolean Logic Unit;

a plurality of input/output interfaces, wherein the plurality of input/output interfaces are operable for receiving a plurality of compiled Boolean expressions/operations and transmitting a plurality of compiled results; and

a plurality of registers, wherein the plurality of registers includes:

a first register for storing the outcome of the most recently evaluated intra-conjunct term,

a second register for storing the outcome of the most recently evaluated conjunct,

an instruction register,

a next operation address register, and

an end of OR address register,

wherein the short-circuit evaluation comprises halting the evaluation of at least a portion of the Conjunctive Normal Form expression/operation if the outcome of the portion becomes known based on an outcome of an evaluation of a prior portion of the Conjunctive Normal Form expression/operation by the Boolean Logic Unit,

wherein the value of the outcome of the prior portion is maintained by the first and second registers, and

wherein the value of the first register will change to a value other than its default value during an intra-conjunct short-circuit operation and force the immediate evaluation of the next conjunct within the current Conjuntive Normal Form expression/operation and forego the evaluation of the remaining terms of the current conjunct if remaining terms exist and the value of the second register will change to a value other than its default value during an inter-conjunct short-circuit operation and forego the evaluation of the remaining portion of the current expression and force the immediate evaluation of the

next Conjunctive Normal Form expression to be evaluated if any remaining Conjunctive Normal Form expressions exist within the instruction store.

2. (cancelled).

3. (Previously Presented) The processor of claim 1, wherein the results of all AND computations in the evaluation of the Conjunctive Normal Form Boolean expression/operation are stored and represented by an *n*-bit AND operation register, wherein the *n*-bit AND operation register is operable for storing the composite results of all conjuncts that have been evaluated at any given point in time during the evaluation of a Conjunctive Normal Form Boolean expression/operation.

4. (Previously Presented) The processor of claim 3, wherein the *n*-bit AND operation register is initialized to a default value.

5. (Previously Presented) The processor of claim 3, wherein the *n*-bit AND operation register initializes to its default value after the start of an operational code.

6. (Previously Presented) The processor of claim 3, wherein the *n*-bit AND operation register remains at its default value if all of the conjuncts of a Boolean expression/operation being evaluated are true.

7. (Previously Presented) The processor of claim 3, wherein the Conjunctive Normal Form Boolean expression/operation is false if the *n*-bit AND operation register is set to any value other than its default value, and the remainder of the Boolean expression/operation is short-circuited.

8. (Cancelled).

9. (Previously Presented) The processor of claim 1, wherein the results of all OR computations in the evaluation of a Conjunctive Normal Form Boolean

expression/operation are stored and represented by an *n*-bit OR operation register, wherein the *n*-bit OR operation register is operable for storing the composite results of all terms that have been evaluated at any given point in time during the evaluation of those terms within any given conjunct in a Conjunctive Normal Form Boolean expression/operation.

10. (Previously Presented) The processor of claim 9, wherein the *n*-bit OR operation register initializes to a default value and remains in that state until a term in a predetermined conjunct evaluates to true.

11. (Original) The processor of claim 10, further comprising an *n*-bit OR conjunct register, wherein the *n*-bit OR conjunct register indicates that the evaluation of a conjunct comprising an OR clause has begun,

12. (Previously Presented) The processor of claim 11, wherein the *n*-bit OR conjunct register initializes to a default value and remains in that state until an expression/operation sets its value to a value other than the default value.

13. (Previously Presented) The processor of claim 11, wherein a predetermined conjunct evaluates to true if the *n*-bit OR register is set to a value other than its default value and the *n*-bit OR conjunct register is set to a value other than its default value, and the processor short-circuits to the start of the next conjunct to be evaluated.

14. (Original) The processor of claim 1, further comprising an operation decoder, wherein the operation decoder is operable for deciphering an operational code and controlling units that are dependent upon the operational code.

15. (Original) The processor of claim 14, wherein functions of the operation decoder comprise Boolean AND, Boolean OR, end of operation, no operation, unconditional jump, conditional jump, start of operation, and start of conjunct.

16. (Original) The processor of claim 1, further comprising a control encoder, wherein the control encoder accepts $n+m$ bits in parallel and outputs them across a device bus either in series or in parallel.

17. (Original) The processor of claim 1, further comprising a random-access memory, wherein the random-access memory is operable for storing the states of a plurality of devices that the processor monitors and controls.

18. (Original) The processor of claim 1, further comprising a memory, wherein the memory is operable for holding a compiled micro-program.

19. (Original) The processor of claim 18, further comprising a program counter, wherein the program counter is operable for fetching an instruction from the read-only memory.

20. (Original) The processor of claim 19, further comprising a memory device, wherein the memory device is operable for configuring the program counter for normal operation, unconditional jump operation, conditional jump operation, and Boolean short-circuit operation.

21. (Original) The processor of claim 1, wherein the plurality of registers comprise a plurality of multi-bit registers.

22. (Original) The processor of claim 21, wherein the plurality of multi-bit registers comprise an instruction register, a next operation address register, and an end of OR address register.

23. (Previously Presented) The processor of claim 22, wherein the instruction register comprises an $n+m+x$-bit wide register comprising an n-bit address, an m-bit control/state word, and an x-bit operational code.

24. (Original) The processor of claim 22, wherein the next operation register stores an address used for Boolean short-circuiting.

25. (Original) The processor of claim 22, wherein the end of OR address register stores the address of an instruction immediately following a conjunct comprising an OR clause.

26. (Original) The processor of claim 1, wherein the plurality of registers comprise a plurality of single-bit registers.

27. (Previously Presented) The processor of claim 26, wherein the plurality of single-bit registers comprise an AND ~~truth state~~ operation register, an OR operation register, and an indicator for conjuncts comprising OR clauses.

Claims 28-45 (cancelled).